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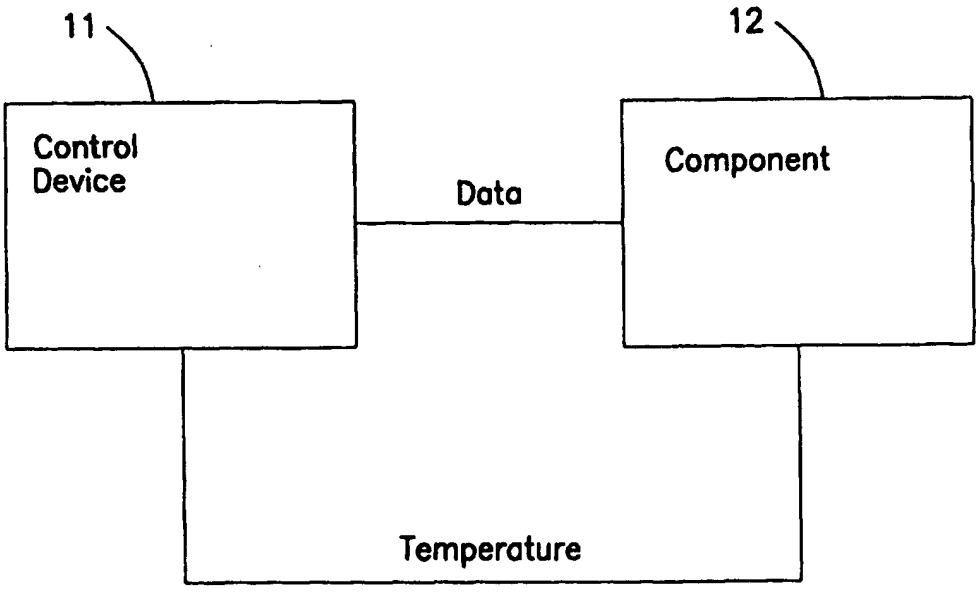
(54) Title: METHOD AND APPARATUS TO CONTROL THE TEMPERATURE OF A COMPONENT



(57) Abstract

When a component, such as a memory device, exhibits an overtemperature condition (e.g., exceeds a first threshold value), the data transmission rate with respect to the component is reduced so as to lower its operating temperature. In one embodiment, this is achieved by changing the latency at which data packets are transmitted to and from the memory device in dependance on the temperature of the device. Controlling temperature in such a fashion allows for efficient use of the component over a large range of temperatures.

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Method and Apparatus to Control the Temperature of a Component

Background of the Invention

The present invention pertains to a method and apparatus to control the temperature of a component. More particularly, the present invention pertains to a method and apparatus to control the temperature in a component by reducing the rate of data transfer to and/or from the component.

Electronic components, such as memory (e.g., Static Random Access Memory (SRAM)), chipsets (e.g., 82430FX PCIset manufactured by Intel Corporation, Santa Clara, California), graphics controllers, and processors (e.g., the Pentium® II processor manufacture by Intel Corporation), are electronic circuits that heat up during operation. In many cases, the specifications for these components indicate a maximum temperature at which the component will operate correctly. If the component exceeds this temperature, several problematic conditions may occur. First, the component may compromise data signals being transferred and/or stored within the component. This leads to errors in other components that rely on such data signals. Also, excessive heat may cause individual circuits in the component to become irreversibly damaged.

Several procedures have been proposed to control overtemperature problems in components such as the electronic components described above. In one system, when a component becomes too hot, it is turned off (i.e., shut down) and requires the user to turn off the computer system and turn it on again (preferably after the component has cooled down).

A problem seen with such a system is that the use of the computer is completely interrupted by the shutting down and turning on of the computer system. There is a need for a method and apparatus that allows for the control of thermal temperature in a component that does not require such an interruption in use.

Summary of the Invention

According to an embodiment of the present invention, an apparatus is provided which controls the temperature of a component. The apparatus includes a control device adapted to be coupled to the component, and adapted to control a data transmission rate between the control device and the component based on a temperature of the component.

Brief Description of the Drawings

Fig. 1 is a general block diagram of a system constructed according to an embodiment of the present invention.

Fig. 2 is a block diagram of an example of the system of Fig. 1.

Figs. 3a-b are block diagrams of a DRAM memory module constructed according to an embodiment of the present invention.

Figs. 4a-4b are flow diagrams of a method according to an embodiment of the present invention.

Detailed Description

Referring to Fig. 1, a general block diagram of an embodiment of the present invention is shown. A control device 11 is provided which transmits data to and/or receives data from a component 12. As used herein the term "data" should be broadly construed so as to include data, command, control, address, and other such signals. Component 12, at least partially as a result of receiving data from control device 11, generates heat during its operation. Component 12 may generate a temperature signal and transmit that signal to control device. For example, this temperature signal could be an actual operating temperature, the exceeding of a predetermined threshold, etc. Based on the temperature signal from component 12, control device 11 reduces the rate at which data is transferred to and/or received from component 12.

Referring to Fig. 2, an example of the circuit of Fig. 1 is shown in a computer system environment. In the embodiment of Fig. 2, computer system 20 includes a processor 21 (e.g., a Pentium® II processor manufactured by Intel Corporation) coupled to a chipset 22 (e.g., 82430FX PCIset manufactured by Intel Corporation). In this example, chipset 22 includes a memory controller hub 22a and an Input/Output (I/O) controller hub 22b. These controllers are sometimes referred to in the art as a "North bridge" and a "South bridge", respectively. Memory controller hub 22a can be coupled to I/O controller hub 22b via a bus 23 (e.g., a bus operating according to the Peripheral Component Interconnect (PCI) specification (Rev. 2.1, PCI Special Interest Group, Hillsboro, Oregon, 1995)). If desired a graphics controller 24 can be coupled to memory controller hub 22a (e.g., via an Advanced Graphics Port (A.G.P.) Interface (see A.G.P. Interface Specification, Revision 1.0, ©1996, Intel Corporation)). Memory controller hub 22a includes a memory status register 31 coupled to a memory

controller 32. Memory controller is coupled to one or more memory devices such as dynamic random access memory (DRAM) devices 33a-c (e.g., Rambus® DRAM devices, Rambus Inc., Mountain View, California).

An example of one of the DRAM devices is shown in Figs. 3a-b. In Fig. 3a, memory device 33a includes a board 41 (such as a printed circuit board (PCB)) upon which are mounted a number of memory modules 42a-d. In this embodiment, a thermal sensor 43 is attached to board 41 (e.g., via bolts). Thermal sensor 43 includes an output signal line 44 (described below). In Fig. 3b, a side view of the memory device 33a of Fig. 3a is shown. In this example, a compressible, thermally conductive elastomer 45 is pressed against the memory modules (e.g., memory modules 42c-d) and thermal sensor 43 with a heat spreader plate 46a. Heat spreader plates 46a-b are made of a suitable thermally conductive material and coupled via pins (e.g., pins 47a-b). In operation, thermal sensor 43 is capable of detecting heat generated by memory modules coupled to board 41 via elastomer 45 and heat spreader plates 46a-b.

In this embodiment, thermal sensor 43 senses the temperature of the memory modules in memory module 33a. For example, thermal sensor 43 can include a known thermistor (i.e., an analog device having a resistance that changes in proportion to ambient temperature) and an analog-to-digital converter that converts the analog voltage value across the thermistor to a digital value (not shown specifically in Fig. 2). The digital value can then be compared to a threshold value (i.e., a value representing a desired maximum operating temperature), and generate a pulse signal on signal line 44 to indicate that the threshold has been exceeded. It may be desirable if the threshold is set to a value lower than the maximum operating temperature set forth in its specification.

In the embodiment of Fig. 2, signal line 44 from sensor 43 is coupled to a general purpose I/O (GPIO) pin on I/O controller hub 22b. Alternatively, thermal sensors on additional memory modules 33b-c may have signal lines (elements 50-51) coupled to this GPIO pin. In that case, signal lines 44, 50, and 51 are used as inputs to an OR gate 55. Accordingly, when an overtemperature condition appears at one or more of memory modules 33a-c (e.g., temperature exceeds a first threshold), an appropriate signal is generated by its corresponding sensor (e.g., sensor 43) and passed through OR gate 55 to the GPIO pin of I/O controller hub 22b. In this example, the overtemperature signal at I/O controller hub 22b causes an interrupt to be generated to processor 21. Examples of appropriate

interrupts include a system management interrupt (SMI) that is present in all Intel Pentium® and Pentium® II processors and a system control interrupt (SCI) (see "Advanced Configuration and Power Interface Specification", Draft Revision 1.0, December 22, 1996, by Intel Corporation *et alia*). In response, processor 21 notifies memory controller hub 22a of the overtemperature condition. In the example of Fig. 2, this is accomplished by writing (or logging) an appropriate value into a memory status register 31.

A memory controller 32 in memory controller hub 22a controls the transmission (e.g., writing and reading) of data to/from DRAM devices 33a-c. In this embodiment, the data is sent and received according to a packet protocol. Each packet is sent based on a latency value (e.g., an amount of time to delay the transmission of the packet to/from DRAM devices 33a-c after the packet has been prepared). For example, during normal operation when DRAM devices 33a-c are not exhibiting an overtemperature condition, the latency value should be low and preferably zero. Memory controller 32 periodically checks the contents of memory status register 31. When register 31 indicates an overtemperature condition in DRAM devices 33a-c, memory controller 32 then increases the latency value, thus slowing down the transmission of data between memory controller hub 22a and DRAM devices 33a-c. The reduction in data traffic to/from DRAM devices 33a-c results in a reduction of the operating temperature for these devices. Accordingly, DRAM devices 33a-c continue to operate (albeit with a slower throughput of data) despite the overtemperature condition rather than being shut down completely. When the data transmission rate is lowered, the transmission of data to DRAM devices 33a-c to/from other devices (e.g., graphics controller 24) may be lowered in response.

When temperature at DRAM devices 33a-c falls below a predetermined second threshold value, another signal (e.g., from sensor 43) is sent to the GPIO pin of I/O controller hub 22b (via OR gate 55) to indicate that these devices are operating at a sufficiently low enough temperature to permit an increase in the data transfer rate with memory controller hub 22a. The receipt of such a signal at I/O controller hub 22a causes a second interrupt to processor 21. In response, processor 21 places the appropriate value in memory status register 31 (e.g., resets the value stored therein). The new value in register 31 causes memory controller 32 to decrease the latency value (e.g., to zero) and increase the data transmission rate between memory controller hub 22a and DRAM devices 33a.

In the embodiment of the present invention described above, DRAM devices 33a-c will continue to operate at an appropriate rate. There is a possibility, however, that the interrupt between I/O controller hub 22b and processor 21 will be impeded. For example, a set of code executed by processor 21 referred to in the art as a virus can disable these interrupts. According to another embodiment of the present invention, other elements can be added to prevent DRAM devices 33a-c from exceeding a maximum rated temperature. I/O controller hub may include a counter that starts counting when a signal is received at the GPIO pin. When counter 60 expires after a predetermined time period, it is determined whether an interrupt has been generated by I/O controller hub 22b. If it has not, then an appropriate message is sent from I/O controller hub 22b to memory controller hub 22a via bus 23 or a dedicated bus 61 between these components. In response, memory controller hub 22a sets the appropriate value in memory status register 31 as indicated in the embodiment described above. When the temperature falls below the second threshold value, the resulting signal at the GPIO pin can be used to immediately generate an appropriate message to memory controller hub 22a or counter 60 can be used to allow I/O controller hub 22b an opportunity to generate the interrupt. As with the example above, the message, received by the memory controller hub 22a, causes the memory status register to reset, thus increasing the data rate to/from DRAM devices 33a-c.

A method according to an embodiment of the present invention is shown in Figs. 4a-4b. In block 101, the system is initialized where it is assumed that all components are operating at an acceptable temperature. Thus, the rate of data transmission to and/or from component 12 (see Fig. 1) is normal (e.g., at full speed). In decision block 103, it is determined whether a component (e.g. component 12 in Fig. 1, or memory such as DRAM memory 33a-c in Fig. 2) is exhibiting an overtemperature condition. If there is no overtemperature, condition control passes back to decision block 103. Otherwise, control passes to block 105 (Fig. 4b) where a counter is optionally started as described above. In block 107 (Fig. 4a), an interrupt is generated (e.g., by I/O controller hub 22b in Fig. 2). In block 109, an overtemperature condition is logged (e.g., by writing appropriate data to memory status register 31 in Fig. 2). In decision block 110 (Fig. 4b), the counter is checked to see if it has expired. If it has, control passes to decision block 111 to determine if an interrupt was generated (e.g., in block 107). If it has not, then the overtemperature condition is logged

in a direct manner (e.g., through direct communication between I/O controller hub 22b and memory controller hub 22a in Fig. 2).

In block 113 (Fig. 4a), the data transmission rate is lowered so as to decrease the operating temperature of component 12 (Fig. 1). In decision block 115, it is determined whether the operating temperature has fallen below a second threshold. In decision block 117 it is determined whether an interrupt was previously generated (e.g., in response to the overtemperature condition in block 107). If it was, then control passes to block 118 (Fig. 4b) where a new interrupt is generated and then an undertemperature condition is logged (e.g., by writing appropriate data to memory status register 31 in Fig. 2; see block 119). If an interrupt was not previously generated, then control passes directly to block 119 to log the undertemperature condition in a direct manner as described above. In block 121, the data rate is increased so as to improve performance.

In the examples of Figs. 1-4, first and second temperature threshold values are used. When a component exceeds the first temperature threshold, the data rate is reduced to a predetermined rate. When the temperature falls below a second temperature threshold, the data rate is increased to its original value. One skilled in the art will appreciate that the method and apparatus shown in Figs. 1-4 can be modified so as to handle additional intermediate threshold values. For example, when temperature exceeds the first (and highest) threshold temperature value, the data transmission rate is reduced to a first (and lowest) value. If the temperature is below the first threshold but exceeds an intermediate threshold temperature (i.e., one that is in between the first and second threshold temperatures), the data transmission rate can be set to a value that is intermediate to the original (full speed) value and the lowest value. Accordingly, using this feature of the present invention, the data transmission rate can be better optimized based on the operating temperature of a component.

Although embodiments are specifically illustrated and described herein, it will be appreciated that modifications and variations of the present invention are covered by the above teachings and within the purview of the appended claims without departing from the spirit and intended scope of the invention. For example, though individual devices are shown in Figs. 1 and 2, many of the devices can be divided into separate components or integrated into larger components. Also, the present invention applies to components other than memory devices. When using a memory device, however, the data transmission rate between the

control device and the memory device can be reduced by reducing number of write operations or read operations per unit time instead of both operations at the same time.

What is claimed is:

1. An apparatus to control temperature of a component comprising:

a control device adapted to be coupled to a component, wherein said control device is adapted to control a data transmission rate between said control device and said component based on a temperature of said component.

2. The apparatus of claim 1 further comprising:

a component coupled to said control device.

3. The apparatus of claim 2 wherein said control device lowers said data transmission rate when the temperature of said component exceeds a first threshold.

4. The apparatus of claim 3 wherein said component is a memory device.

5. The apparatus of claim 4 wherein said control device is a memory controller hub.

6. The apparatus of claim 5 wherein said memory controller hub includes a memory controller, said memory controller is adapted to transmit data packets to said memory device with an amount of latency, said latency amount being increased when a temperature of said memory device exceeds said first threshold.

7. The apparatus of claim 6 wherein said latency amount is decreased when a temperature of said memory device falls below a second threshold.

8. An apparatus to control temperature of a memory device comprising:

a memory device including:

at least one memory module; and

a temperature sensor coupled to said memory module.

9. The apparatus of claim 8 wherein said memory device further includes

a board where said memory module and said temperature sensor are coupled to said board.

10. The apparatus of claim 9 wherein said memory device further includes

a thermally conductive elastomer coupled to said memory module and said temperature sensor.

11. The apparatus of claim 10 further comprising:

a control device coupled to said memory device, said control device is adapted to control a data transmission rate between said control device and said component based on a temperature of said component.

12. The apparatus of claim 11 wherein said control device lowers said data transmission rate when the temperature of said memory device exceeds a first threshold.

13. The apparatus of claim 12 wherein said control device is a memory controller hub.

14. The apparatus of claim 13 wherein said memory controller hub includes a memory controller, said memory controller is adapted to transmit data packets to said memory device with an amount of latency, said latency amount being increased when a temperature of said memory device exceeds a first threshold.

15. The apparatus of claim 14 wherein said latency amount is decreased when a temperature of said memory device falls below a second threshold.

16. A method of controlling temperature in a component comprising:

controlling a data transmission rate between a control device and said component based on a temperature of said component.

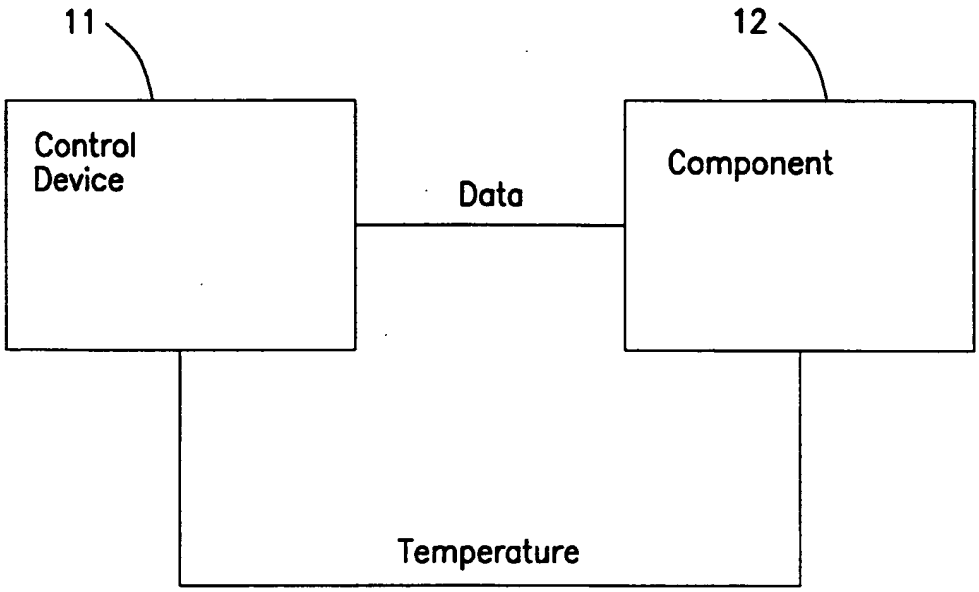
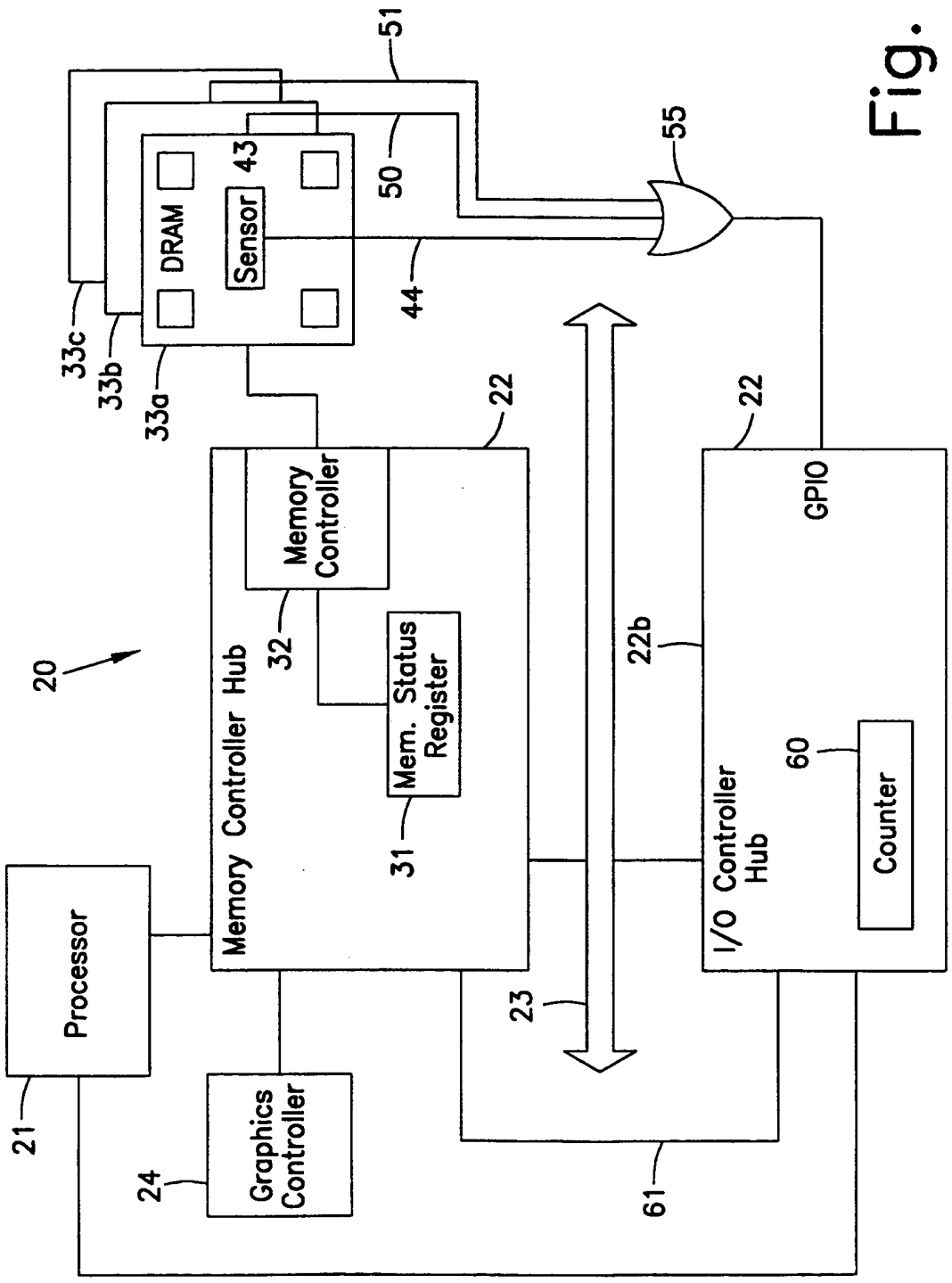


Fig. 1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55
50
43
DRAM
Sensor
44
33c
33b
33a
22
22
Memory Controller
GPIO
20
32
22b
Mem. Status Register
Memory Controller Hub
I/O Controller Hub
60
Counter
31
Processor
23
Graphics Controller
21
24
61

Fig. 2

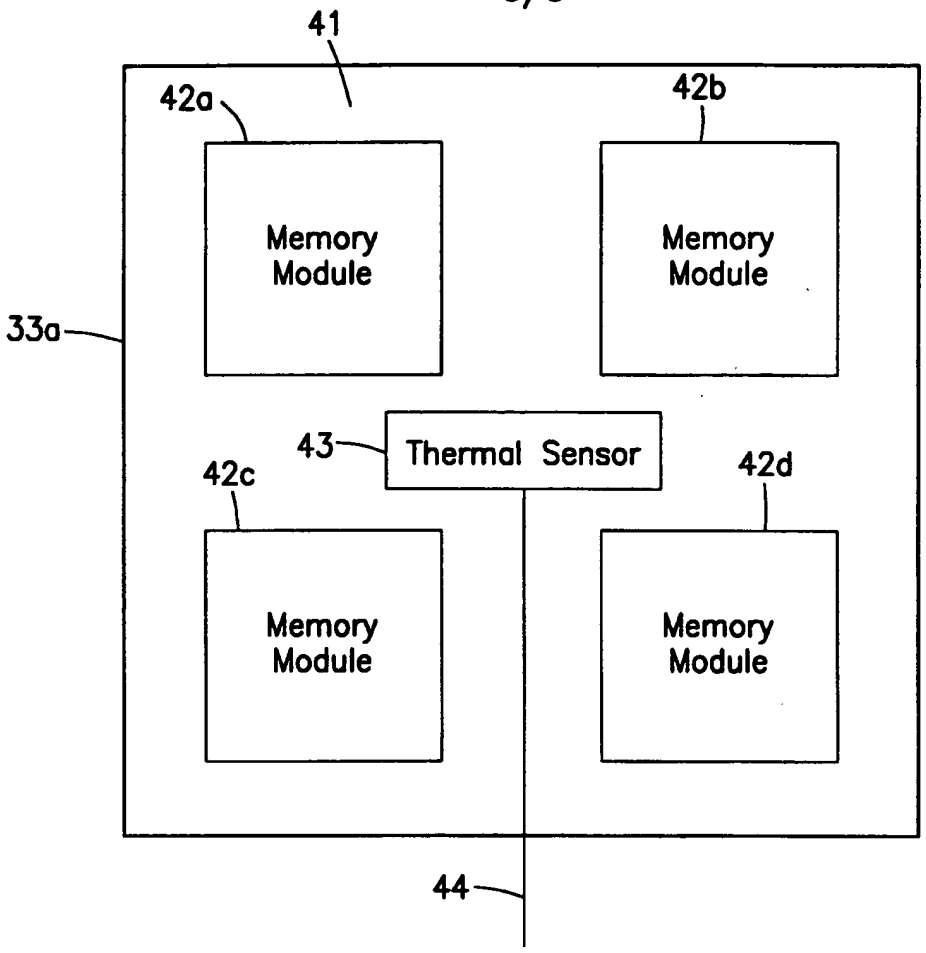

41
42a
42b
Memory Module
Memory Module
33a
43
Thermal Sensor
42c
42d
Memory Module
Memory Module
44

Fig. 3a

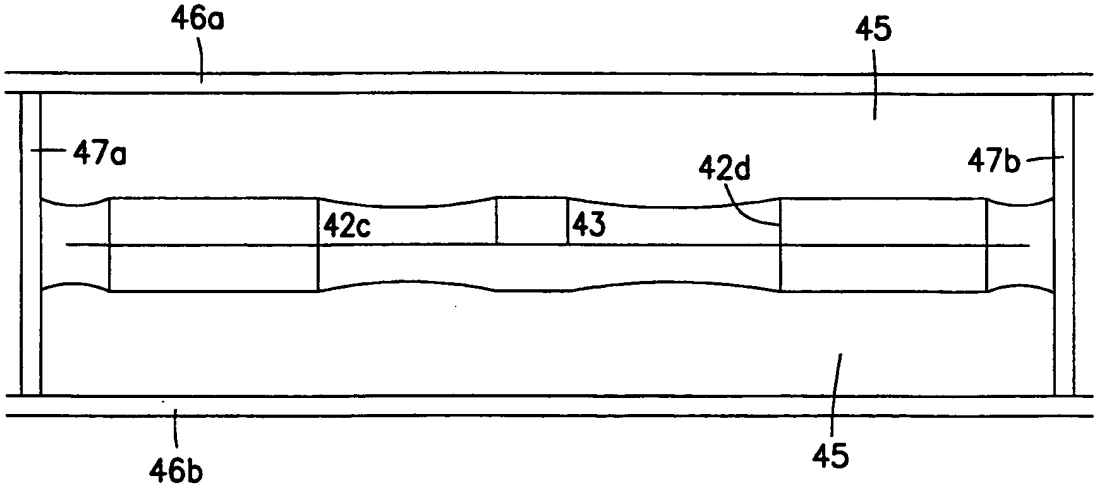

46a
45
47a
47b
42d
42c
43
46b
45

Fig. 3b

Fig. 4a

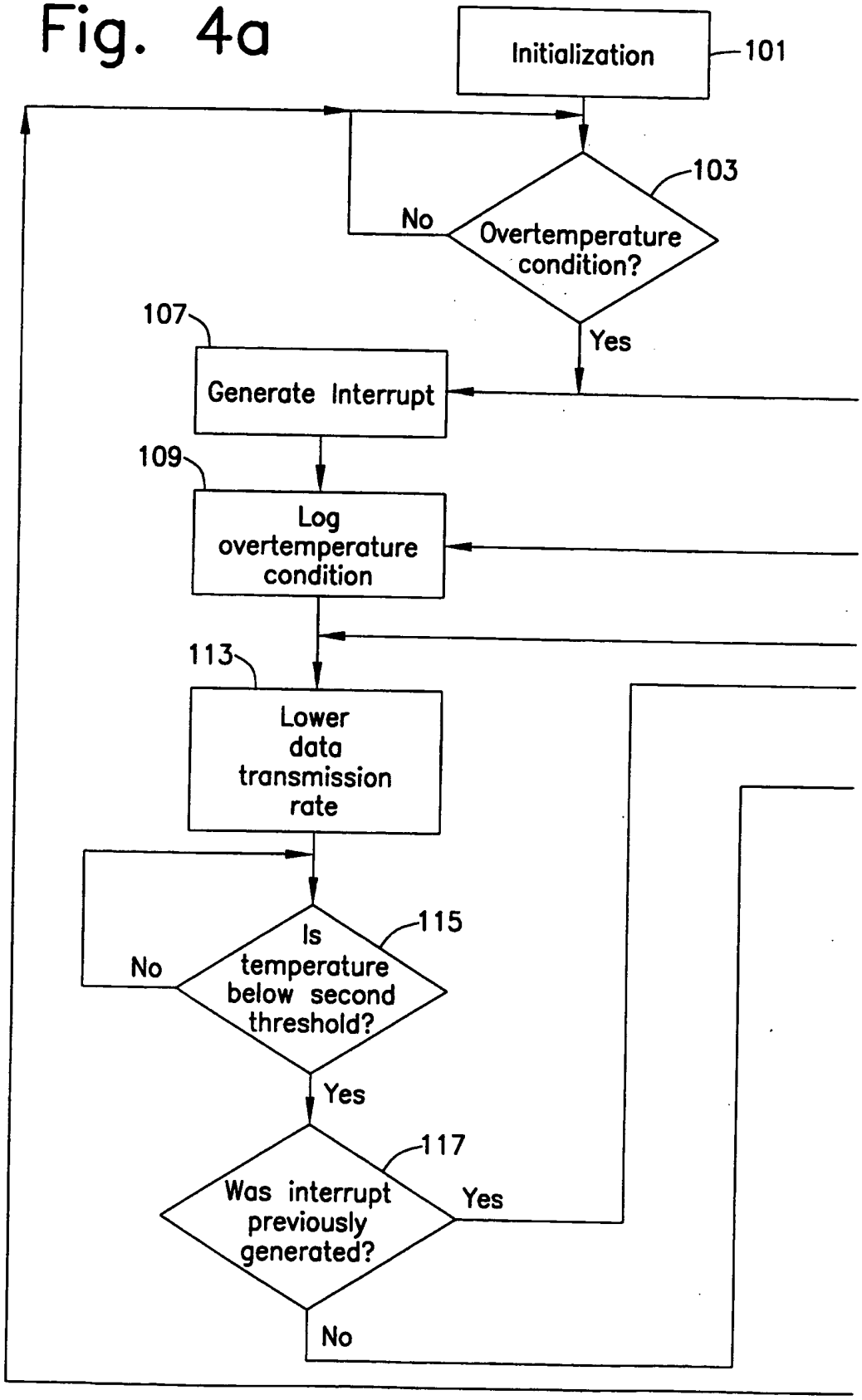
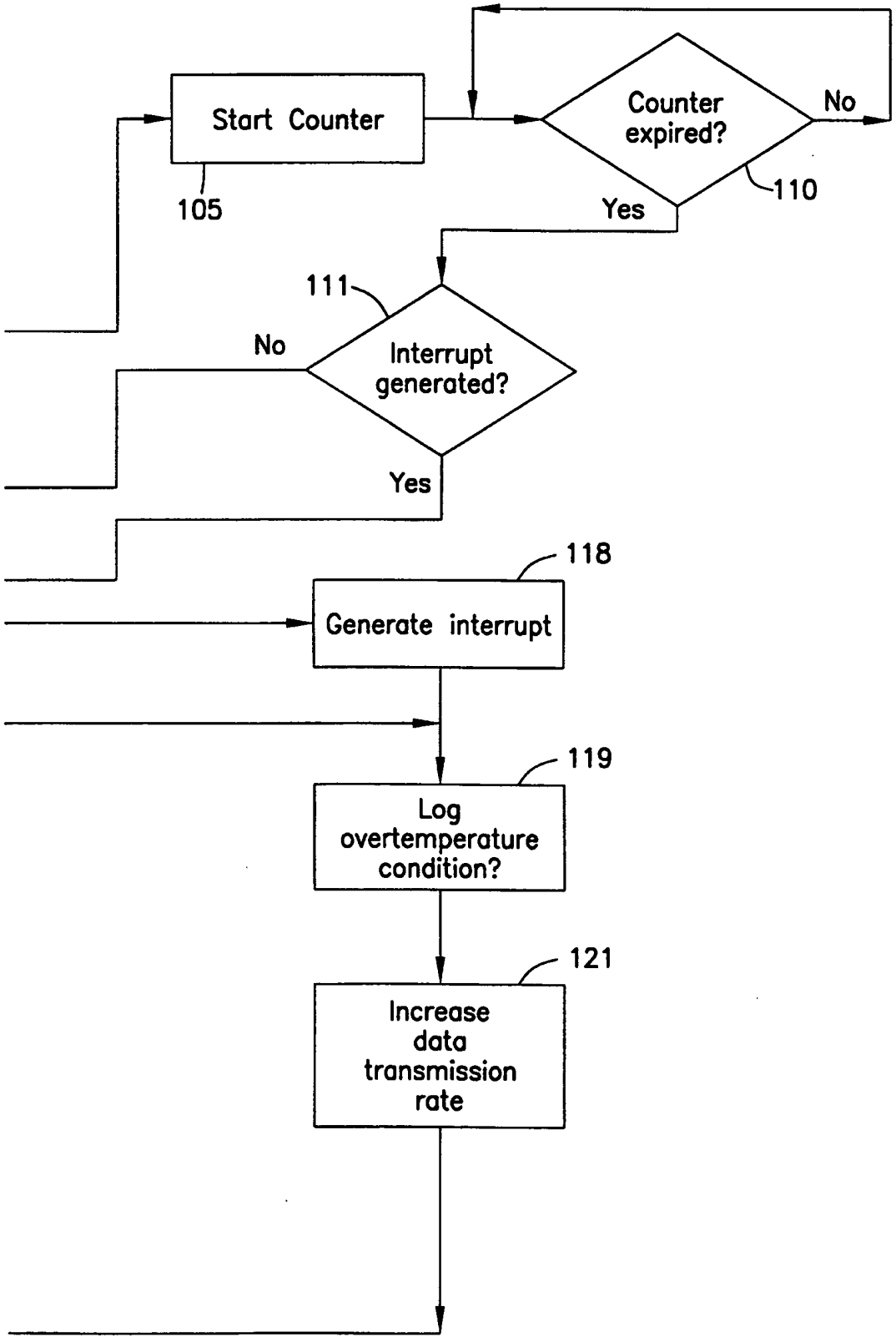

Initialization
101
103
No
Overtemperature condition?
Yes
107
Generate Interrupt
109
Log overtemperature condition
113
Lower data transmission rate
115
No
Is temperature below second threshold?
Yes
117
Was interrupt previously generated?
Yes
No

Fig. 4b


Start Counter
105
Counter expired?
No
110
Yes
111
Interrupt generated?
No
Yes
118
Generate interrupt
119
Log overtemperature condition?
121
Increase data transmission rate

INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/US 99/18433

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C7/00

According to International Patent Classification (IPC) or to both national classification and IPC

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Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 276 843 A (TILLINGHAST CHARLES W ET AL) 4 January 1994 (1994-01-04) column 4, line 21-32; figures 1,2	1-16
X	US 5 446 696 A (WARE FREDERICK A ET AL) 29 August 1995 (1995-08-29) claims 9,10; figure 5	1-16
X	EP 0 851 427 A (LSI LOGIC CORP) 1 July 1998 (1998-07-01) figures 1,2	1-5, 8-13,16

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29 September 1999	06/10/1999

Name and mailing address of the ISA	Authorized officer
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Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5276843 A	04-01-1994	NONE	
US 5446696 A	29-08-1995	AU 6988494 A	20-12-1994
		JP 9501254 T	04-02-1997
		WO 9428553 A	08-12-1994
EP 0851427 A	01-07-1998	US 5784328 A	21-07-1998
		JP 10255467 A	25-09-1998